ABSTRACT

A low cost technique for packaging microelectronic circuit chips fixes a die within an opening in a package core. At least one metallic build up layer is then formed on the die/core assembly and a grid array interposer unit is laminated to the build up layer. The grid array interposer unit can then be mounted within an external circuit using any of a plurality of mounting technologies (e.g., ball grid array (BGA), land grid array (LGA), pin grid array (PGA), surface mount technology (SMT), and/or others). In one embodiment, a single build up layer is formed on the die/core assembly before lamination of the interposer.